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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,362	11/13/2001	Maged E. Beshai	14880ROUS01U	7035

34845 7590 10/21/2005

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EXAMINER	
CHO, HONG SOL	

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,362	BESHAI ET AL.	
	Examiner	Art Unit	
	Hong Cho	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-28 and 32* is/are allowed.

6)☒ Claim(s) *29-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 April 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04032002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. New corrected drawings are required in this application because legends are not complete for figures 1, 2, 20, 24, 29, 30 and 32. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(e) that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 29 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Handelman (USPUB 20030043430).

Re claim 29, Handelman discloses optical packet switch with switching fabric including a plurality of input and output ports for switching fixed-length and variable length optical packets (*a core node having a plurality of space switches, each space switch having burst-mode input ports and channel-mode input ports*, paragraph [0081]; figure 1). Handelman discloses switching burst data packets to the output ports (each burst-mode input port switches individual data bursts to respective output ports, paragraph [0118], lines 4-5). Handelman discloses passive switching node receiving optical packets from more than one input port or output port over more than one channel wavelength and outputting optical packets to one or more of the plurality of output ports (*each channel-mode input port has a switched channel connection carrying a succession of data units of any format to a single output port,* paragraph [0152]).

Re claim 30, Handelman discloses selecting the optical channel for a inputted optical packet and switching the optical packet over one of the groups of wavelengths that is matched to the one inputted optical packet by correspondence of attributes of the at least one packet characteristic (*the search for a channel connection starts from the same space switch and follows the same order for each channel connection and wherein the number of channel connections in a space switch is limited below a predetermined upper bound*, paragraph [0192]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Handelman.

Re claim 31, Handelman discloses all of the limitations of the base claim, but fails to disclose allocating the burst connections equitably among the space switches. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify switching/routing control unit of Handelman to determine the same number of groups of wavelengths for switching optical packets so that each space switch would switch burst traffic at constant rate.

Allowable Subject Matter

6. Claims 1-28 and 32 are allowable.

The following is an examiner's statement for reasons for allowance.

7. Claim 1 is allowable over the prior art of record since the cited references taken individually or in combination fail to particularly teach or fairly suggest a burst-switching network comprising a plurality of source nodes, a plurality of upstream links coupled to said plurality of source nodes, a plurality of sink nodes, a plurality of downstream links coupled to said plurality of sink nodes, a plurality of core nodes, at least one of said plurality of core nodes is coupled to a subset of said plurality of upstream links and a

subset of said plurality of downstream links and has a plurality of space switches, each space switch having a slave controller, and a plurality of master controllers in each core node, one said master controller associated with each of said plurality of space switches in each of said plurality of core nodes and a designated one of said master controllers in a core node functions as a core-node controller, said core-node controller communicatively connecting to each of said master controllers, said core-node controller operable to receive control data from at least one of said plurality of source nodes, divide said control data among said master controllers, and instruct each master controller to generate a burst-switching schedule for a space switch associated with said each master controller, communicate said schedule to a respective edge node, and transmit instructions based on said schedule to a slave controller of said space switch after a pre-calculated delay period.

Claim 10 is allowable over the prior art of record since the cited references taken individually or in combination fail to particularly teach or fairly suggest a bufferless space switch having a plurality of burst-mode input ports and a plurality of output ports, a method of determining a schedule for switching data bursts, over a designated schedule period T, from said plurality of burst-mode input ports to said plurality of output ports, the method including the step of repetitively employing said schedule for switching data bursts during m consecutive periods, m being an integer greater than zero and each of said consecutive periods is equal to said designated period.

Claim 16 is allowable over the prior art of record since the cited references taken individually or in combination fail to particularly teach or fairly suggest a bufferless space switch having a plurality of burst-mode input ports and a plurality of output ports, a

method of determining a schedule for switching data bursts, over each of successive time intervals, each time interval having a duration T, from said plurality of burst-mode input ports to said plurality of output ports, comprising the steps of setting the computation period for each of said successive time intervals to an integer multiple m of the interval T, and computing m successive schedules concurrently.

Claim 20 is allowable over the prior art of record since the cited references taken individually or in combination fail to particularly teach or fairly suggest a method of computing a burst-switching schedule in a bufferless space switch having a plurality of burst-mode input ports by receiving burst descriptors associated with each of the plurality of burst-mode input ports, placing said burst descriptors in bursts queues, at least one queue being associated with each one of said plurality of burst-mode input ports, cyclically accessing said burst queues, determining corresponding input free time and selecting a maximum of Q candidate burst descriptors, determining free time for output port indicated in each candidate burst descriptor, determining the absolute value W of the difference between the output-free time corresponding to each of the Q burst descriptors and said input free time, and selecting the candidate burst yielding the least value W.

Claim 24 is allowable over the prior art of record since the cited references taken individually or in combination fail to particularly teach or fairly suggest A burst scheduler for a space switch, said space switch having a plurality of input ports and a plurality of output ports, said scheduler including: a receiver for receiving burst descriptors and placing each of said burst descriptors in one of a plurality burst-descriptor memories, each of said burst descriptors identifying an input port, an output port, and a

burst size, an input-state memory for storing next available time of each of said input ports; a plurality of output-state memories, each storing next-available time of each of said output ports, a processing circuit including a scheduler kernel for computing a schedule for burst- transfer across said space switch over a predefined period of time T, said processing circuit operable to select a number Q of candidate burst descriptors for each input port, where Q is an integer greater zero, compare corresponding entries in said input-state memory and said plurality of output-state memories for each of said Q candidate burst descriptors and determine a corresponding merit index; and select one of said Q candidate burst descriptors according to said merit index; and a permits buffer for storing said schedule.

Claim 32 is allowable over the prior art of record since the cited references taken individually or in combination fail to particularly teach or fairly suggest a core node having a plurality of space switches operated in parallel, each of said plurality of space switches having a plurality of input ports, a plurality of output ports, and a master controller with one said master controller designated to function as a core-node controller, said core node switching burst streams from a plurality of upstream links, each having multiple wavelength channels, to a plurality of downstream links, each having multiple wavelength channels, a method of confining connections from each upstream link to each downstream link to a small number of space switches, the method comprising the steps of receiving a bitrate requirement for each connection, sorting received bitrate requirements associated with each upstream link in a descending order according to bitrate value, implementing a cyclic allocation of said requirements to

corresponding paths of the space switches, retaining a remainder when one of said corresponding paths is exhausted, and determining a progress indicator, and repeating said cyclic allocation if permitted by said progress indicator.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US Patent (6021086) to Joffe
- US Patent (6118762) to Nomura et al

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Cho whose telephone number is 571-272-3087. The examiner can normally be reached on Mon-Fri during 7 am to 4 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571-272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-3088.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

hc

Hong Cho
Patent Examiner
10/13/2005

JOHN PEZZLO
PRIMARY EXAMINER